WHAT IS CLAIMED IS:

- 1 1. A method of passing N-bit word data over an M-bit channel, M being less than N,
- 2 each N-bit word having a first portion and a second portion, the method comprising:
- 3 transferring the first portion of each of X words in M-bit groups, X being at least two;
- 4 and
- transferring at least one other bit group, the at least one other bit group including bits
- 6 from the second portions of at least two of the X words.
- 1 2. The method of claim 1, further comprising:
- 2 joining, for each of the X words, the second portion to the corresponding transferred
- 3 first portion, the second portion being extracted from the transferred at least one other bit
- 4 group.
- 1 3. The method of claim 1, wherein the first portion includes M bits of encoded
- 2 information, and the second portion includes encoding information.
- 1 4. The method of claim 3, wherein the second portion further includes DC content
- 2 balancing information.
- 1 5. The method of claim 3, wherein N is 10, M is 8.
- 1 6. The method of claim 5, wherein the M-bit channel includes a Digital Visual Interface
- 2 (DVI) portion.
- 7. The method of claim 5, wherein the first portion is a most-significant bits portion, and
- 2 the second portion is a least-significant bits portion.

US018182 (VLSI.332PA)

- 1 8. The method of claim 1, wherein the first portion is a most-significant bits portion, and
- 2 the second portion is a least-significant bits portion.
- 1 9. The method of claim 1, wherein the first portion is a least-significant bits portion, and
- 2 the second portion is a most-significant bits portion.
- 1 10. The method of claim 1, wherein X is an integer and multiple of M/(N-M).
- 1 11. The method of claim 10, wherein X is 4.
- 1 12. The method of claim 1, wherein the bit-length of the first portion is an integer multiple
- 2 of M.
- 1 13. The method of claim 1, wherein the bit-length of the second portion is less than M.
- 1 14. The method of claim 1, further comprising storing the N-bit word data in X locations
- 2 at a first rate, each location being N-bits wide, wherein each N-bit word is stored in one of the
- 3 X locations, and transferring includes reading from the X locations at a second rate, the
- 4 second rate being faster than the second rate.
- 1 15. The method of claim 1, wherein the at least one other bit group includes M bits.
- 1 16. The method of claim 1, further comprising arranging for transfer the N-bit word data
- 2 at a first rate, wherein transferring is at a second rate, the second rate being at least as fast as
- 3 the first rate.
- 1 17. The method of claim 16, wherein the second rate is faster than the first rate.
- 1 18. The method of claim 16, wherein the second rate is N/M times faster than the first rate.

- 1 19. The method of claim 16, wherein the first portion of each of X words are transferred in
- 2 a sequence corresponding to an order by which each of X words was provided.
- 1 20. The method of claim 1, further comprising:
- 2 arranging for transfer X N-bit words in a first storage element; and
- arranging for transfer, while transferring the first portion of each of X words and at
- 4 least one other bit group, another X N-bit words in another storage element.
- 1 21. The method of claim 20, further comprising:
- 2 for each of the X words, joining the second portion to the corresponding transferred first
- 3 portion, the second portion being extracted from the transferred at least one other bit group.
- 22. An apparatus for passing N-bit word data over an M-bit channel, M being less than N, each N-bit word having a first portion and a second portion, comprising:
- 2 means for transferring the first portion of each of X words in M-bit groups; and
- means for transferring at least one other bit group, the at least one other bit group
- 4 including bits from the second portions of at least two of the X words.
- 1 23. The apparatus of claim 22, further comprising:
- 2 means for joining, for each of the X words, the second portion to the corresponding
- 3 transferred first portion, the second portion being extracted from the transferred at least one
- 4 other bit group.
- 1 24. The apparatus of claim 22, further comprising means for storing the N-bit word data in
- 2 X locations at a first rate, each location being N-bits wide, wherein each N-bit word is stored
- 3 in one of the X locations, and transferring includes reading from the X locations at a second
- 4 rate, the second rate being faster than the second rate.

- 1 25. The apparatus of claim 22, further comprising means for arranging for transfer the N-
- 2 bit word data at a first rate, wherein transferring is at a second rate, the second rate being at
- 3 least as fast as the first rate.
- 1 26. The apparatus of claim 22, further comprising:
- 2 means for arranging for transfer X N-bit words in a first storage element; and
- means for arranging for transfer, while transferring the first portion of each of X words
- 4 and at least one other bit group, another X N-bit words in another storage element.
 - 27. A apparatus for passing N-bit word data over an M-bit channel, M being less than N,
- each N-bit word having a first portion and a second portion, comprising:
- a first circuit arrangement adapted to transfer the first portion of each of X words in
- 3 M-bit groups; and
- a second circuit arrangement adapted to transfer at least one other bit group, the at
- 5 least one other bit group including bits from the second portions of at least two of the X
- 6 words.
- 1 28. The apparatus of claim 27, further comprising:
- 2 a receive circuit arrangement adapted to join, for each of the X words, the second
- 3 portion bits to the corresponding transferred first portion, the second portion bits being
- 4 extracted from the transferred at least one other bit group.
- 1 29. The apparatus of claim 27, further comprising a storage element adapted to store the
- 2 N-bit word data in X locations at a first rate, each location being N-bits wide, wherein each N-
- 3 bit word is stored in one of the X locations, and transfer includes reading from the X locations
- 4 at a second rate, the second rate being faster than the second rate.

US018182 (VLSI.332PA)

- 1 30. The apparatus of claim 27, further comprising another circuit arrangement adapted to
- 2 arrange for transfer the N-bit word data at a first rate, wherein transferring is at a second rate,
- 3 the second rate being at least as fast as the first rate.
- 1 31. The apparatus of claim 27, further comprising:
- 2 a circuit arrangement adapted to arrange for transfer X N-bit words in a first storage
- 3 element; and
- a circuit arrangement adapted to arrange for transfer, while transferring the first
- 5 portion of each of X words and at least one other bit group, another X N-bit words in another
- 6 storage element.